SERIAL NO. 09/505748

PATENT
Docket RAL9-99-0181

CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))
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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re application of Raj K. Singh, et al.	:	Date: November 9, 2004 IBM Corporation - IP Law 9CCA/B002
	:	P.O. Box 12195
Serial No. 09/505748	:	Research Triangle Park, North Carolina 27709
Filed: 2/16/2000	:	Customer Number 25299
For: CUSTOMIZABLE SIMULATION MODEL OF AN ATM/SONET FRAMER FOR SYSTEM LEVEL VERIFICATION AND PERFORMANCE CHARACTERIZATION	:	Unit: 2123 Examiner: Kandasamy Thangavelu

APPEAL BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection of claims 1-3, 6 and 13-17 of this application. An appendix containing a copy of the claims is attached.

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I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation (IBM), Assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 4, 5 and 7-12 have been canceled.

Claims 1, 2, 3, 6 and 13-17 are on appeal.

IV. STATUS OF AMENDMENT

No amendment has been filed subsequent to the Final Rejection.

V. SUMMARY OF INVENTION

The present invention provides architecture and implementation of a behavioral VHDL (Verilog) model of a ATM/SONET framer.

Figure 1 shows a graphical representation of the framer 102 including a receiver (Rx) section (left side of Figure 1) and a transmitter (Tx) section (right side of Figure 1). The combination offers flexibility to allow testing with framers from

multiple vendors by changing programmable parameters of the model. Applicants specification, page 2, lines 13-19. An interface termed "UTOPIA" (Universal Test and Operations PHY) using ATM protocol couple's the framer to a unit under test. Likewise, an interface termed "SONET" (Synchronous Optical Network), using SONET protocols couple the framer at various SONET line rates, such as 155.52 Mbps (OC-3), 622.08 Mbps (OC-12), 2488.32 Mpbs (OC-48) etc, to the network. The UTOPIA (ATM) and SONET interfaces use different clock frequencies and thus, represent two distinct clock domains 103 and 104.

The transmitter section 105 of the framer includes UTOPIA slave Tx interface, a first set (0-15) of FIFO buffers, SONET framer processes and a second set (0-15) of FIFO buffers. The function provided by each of the named features are set forth at page 8, lines 25 through page 10, line 8, applicants specification.

The Receiver section of the framer is at left of the transmitter section Figure 1. It contains like elements arranged in opposite orientation to those in the transmitter section. Description of the Receiver section is set forth on page 12, lines 12 through page 14, lines 10, applicants specification.

VI. ISSUES

A. Whether Claims 1, 13 and 3 are unpatentable under 35 U.S.C 103 (a) over **Seawright et al. (SE)** (U.S. Patent 5,920,711) in view of **Kim et al. (KI)** (IEEE, August 1999), **Koziotis et al. (KO)** (IEEE, October 1999), **Karr et al. (KA)** (U.S. Patent 6,668,297), **Kim et al. (KIM)** (U.S. Patent 5, 978,377), and further in view of **Zwan et al. (ZW)** (U.S.

Patent 5,991, 270).

B. Whether Claim 2 is unpatentable under 35 U.S.C 103 (a) over **Seawright et al.** (**SE**) (U.S. Patent 5,920,711) in view of **Kim et al.** (**KI**) (IEEE, August 1999), **Koziotis et al.** (**KO**) (IEEE, October 1999), **Karr et al.** (**KA**) (U.S. Patent 6,668297), **Kim et al.** (**KIM**) (U.S. Patent 5, 978,377), and further in view of **Zwan et al.** (**ZW**) (U.S. Patent 5,991, 270), and further in view of **Bagheri et al.** (**BA**) (IEEE, May 1995).

C. Whether Claim 6 is unpatentable under 35 U.S.C 103 (a) over **Seawright et al.** (**SE**) (U.S. Patent 5,920,711) in view of **Kim et al.** (**KI**) (IEEE, August 1999), **Koziotis et al.** (**KO**) (IEEE, October 1999), **Karr et al.** (**KA**) (U.S. Patent 6,668,297), **Kim et al.** (**KIM**) (U.S. Patent 5, 978,377), **Zwan et al.** (**ZW**) (U.S. Patent 5,991, 270), and **Bagheri et al.** (**BA**) (IEEE, May 1995), and further view of **Johnston et al.** (**JO**) (IEEE, June 1991), **Morrian** (**MO**) (U.S. Patent 6,415,325), and **Platt** (**PL**) (U.S. Patent 5,802,073)

D. Whether Claims 14-16 is unpatentable under 35 U.S.C 103 (a) over **Seawright et al.** (**SE**) (U.S. Patent 5,920,711) in view of **Kim et al.** (**KI**) (IEEE, August 1999), and **Koziotis et al.** (**KO**) (IEEE, October 1999), and further in view of **Kim et al.** (**KIM**) (U.S. Patent 5, 978,377).

VII. GROUPING OF CLAIMS

There are four groups of claims.

Group 1 consists of Claims 1,13 and 3. The claims of this group do not stand for fall together.

Group 2 consists of Claim 2.

Group 3 consists of Claim 6.

Group 4 consists of Claims 14-16. The claims do not stand or fall together.

VIII ARGUMENTS

Issues and related arguments are identified by the same alphabetical characters.

A. The arguments supporting patent ability of claims 1, 13, and 3 follow:

A1. Examiner Erred in Construing US Patent 5,920,711

Claim 1 calls for " means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors," It is applicant's contention this element and preamble of claim; calling for an ATM/SONET Framer are not disclosed or suggested in U.S. Patent 5,920,711 (hereafter Seawright et al.). Instead, Seawright et al. discloses a system

or a tool set for specifying, synthesizing and simulating a generic protocol using a graphic user interface (GUI). The user uses the GUI to generate a high level description language (HDC) that reflects the specified protocol. The invention translates the protocol into a "virtual circuit" which can be linked to conventional simulator software via interface called "SIMPLUG." See summary of the invention, Seawright et al.

In addition, to not disclosing the above elements of applicants claim, Seawright et al. disclose a different invention from the invention claimed by applicants. Applicant's invention relates to a simulation model of an ATM/SONET Framer whereas Seawright et al. relates to a tool that generates and synthesis circuit based upon frame protocol. It is applicants contention these are different inventions and the teachings in Seawright et al. does not suggest applicants claimed invention.

Applicants take notice of the Examiner's position that Seawright et al disclose the elements of applicants claim set forth above. In particular, the Examiner identified specific sections (see Final Office Action, Paper # 9, Page 3, Last line) of Seawright et al. to support his position. Applicants respectfully disagree with the Examiner. It appears as if the Examiner misconstrued the teachings of Seawright et al. For example, the Examiner relied on abstract L4-10 of Seawright et al. L4-10 of the abstract reads:

> "The GUI also allows the user to analyse an intermediate virtual circuit resulting from the protocol and to check the syntax of the protocol specification. In addition, the GUI allows the user to generate a High-Level Description Language (HDL) file for the protocol. After the HDL is generated, the user can,

through the GUI, simulate the operation of the HDL."

It is clear that this language does not teach or suggest " the above stated element of applicants' claim, which, in part reads: behavioural model that offer sufficient parameters which can be programmed to represent Framers from different vendors." Likewise, the other sections of the reference relied in by the Examiner do not appear to teach this element of Claim 1.

A2. US Patent 5,991,270 Does Not Teach "... Transmitter System and Receiver System ... each includes a UTOPIA interface programmable to provide different protocol"

Claim 1, element 3, in part calls for Transmitter and Receiver each includes UTOPIA interface programmable to provide different protocols. US Patent 5,991,270 to Byron J. Zwan (herein after Zwan) discloses a single integrated testing device to test different type format in a single platform. The test device consists of a plurality of test modules for DSI, DS3, SONET and ATM couple to a switch matrix (See figure 1 and summary of invention). No where in Zwan is a teaching or suggestion of this element of applicants Claim 1. Therefore, it appears as if the Examiner misconstrued Zwan and erroneously concludes that it teaches the element of applicants Claim 1.

The Examiner relied on teachings at Col. 1 lines 35-41 and Abstract of Zwan basis for his position (see first paragraph, page 5, Final Office Action, Paper # 9).

Applicants respectfully disagree with the Examiner and argue that the teaching relied

on by the Examiner merely set forth what the inventor (Zwan) deemed desirable. The system (see description above in this section) which Zwan designed and developed to meet what he deemed desirable is different from this claim element of applicants invention. The fact that Zwan provides a different system to carry out what he considered desirable is evidence that the reference does not suggest the claimed element. Therefore, the Examiner's reliance on Zwan (ZW) appears to be misplaced.

A3. Chan Kim et al. Does Not Disclose SONNET Framer Processes including a Format Translator

The penultimate element of applicants' Claim 1 calls for " SONET Framer Processes including a format translator." This element of applicants Claim 1 is not shown in Kim et al. article (IEEE, August 1999) the Examiner (in Final Office Action, Paper # 9, Page 3) identify this article as KI at page 6, first paragraph, same Final Office Action. The Examiner relied of Kim (KI) to teach this element of applicants Claim 1.

A review of KI, clearly shows it does not teach this element. Instead, KI teaches design and simulation of three ATM ASICS. One of the ASIC termed " ASAH_NIC" is an ATM SAR chip with PCI core and SDH framer. (See Kim article 2 Col. 1). The framer performs 155 Mbps ATM physical layer processing including all rate adaptation etc (see Kim Col. 2 lines 12-17). Applicants could not find any reference to SONET much less teachings of SONET framer ... recited in Claim 1. As a consequence applicants contend the Examiner appears to erred and erroneously conclude this element of applicants Claim 1 is disclosed in the prior art.

A4. Examiner Fails to Make Out Prima Facie Case of Obviousness With Respect to Claims 1, 13 and 3

Claims 1, 13 and 3 are rejected under 35 U.S.C. 103 (a) obviousness. The Examiner combine six (6) references in rejecting these Claims.

To establish a prima facie case obviousness three (3) basic criteria must be met.

First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art references when combined must teach or suggest all the claim limitations. MPEP2143

It is applicants contention based upon arguments set forth herein none of the criteria has been met. Therefore, Claims 1, 13 and 3 are patentable without applicants providing any evidence of un-obviousness.

A5. No Suggestion or Motivation to Combine is Found in Any of the References

Applicants Claim1 has six (6) elements and the Examiner has combined six (6) references to reject it under 35 U.S.C. 103 (a). It is settled law that in order to reject a claim based upon a combination of references at least one of the references should suggest motivation for combining. A review of the six references did not find any suggestion to combine. In Addition, the Examiner did not identify teachings in the references that suggest the combination. Therefore, it appears as if the combination is improper.

Even though there is no suggestion or motivation to combine in the references, the Examiner could still combine them provided the combination is based upon knowledge generally available to one of ordinary skill in the art. A review of the reasons for the combination set forth in the Office Action seem to indicate the Examiner is relying on the knowledge generally available to one of the ordinary skill in the art form the combination.

In this regard applicants contend the Examiner's arguments for combination are too complex to be characterized as arguments based upon knowledge generally available to one of ordinary skill in the art. The knowledge generally available to someone of ordinary skill in the art should be limited to knowledge possess by one having an Associates Degree which is usually obtain after two years attendance at a community college or junior college. It should not be the knowledge possess by a PHD. It should be noted that the Examiner refers to himself as Dr. which suggest he has a PHD. To use arguments based upon knowledge of a PHD would not be knowledge of someone skilled in the art a requirement of the patent statute. In other words, arguments in support of combination based upon knowledge of a PHD appears extraordinary and should be rejected out of hand. An example of this complexity of the Examiner's argument is given at page 6, first full paragraph of the Final Office Action Paper #9. In view of the above Claims 1, 13 and 3 are patentable over the art of record.

A6. No Reasonable Expectation of Success for the Combination

One of the criteria for making out a prima facie case of obviousness is that there must be a reasonable expectation of success.

It is applicants contention a reasonable expectation of success is not present in this

case. Because the teachings of the individual reference are too diverse for one to reasonably expect success in their combination. For example, Seawright et al. (US Patent 5,920,711) the primary reference discloses a system having a GUI in which a user input protocol information. The system generates a virtual circuit which can be applied to a simulator through an interface termed "SIMPLUG." One of the secondary references entitled " O.6um CMOS, 622/155 Mbit/s ATM_ SDH/SONET framer 1C" by M.Koziotis et al. teaches a framer that maps ATM cell into SONET format frames. It is applicants contention synthesizing a virtual circuit (Seawright et al.) and converting ATM cell into SONET format are different with no reasonable expectation of success when combined. Therefore, this criteria is not met and Claims 1, 13 and 3 are not obvious.

A7. Examiner's Combination Fails to Teach all of the Claims_Limitations

Finally, to make out a prima facia case of obviousness every limitation of the claim must be found in the combination. As argued in A1, A2 and A3 incorporated herein by references, the identified elements, single or in combination, is not found or present in the Examiner's combination. Therefore, even after the combination the named elements are not present. As a consequence this criteria is not met and the Claims 1, 13 and 3 are not obvious.

A8. Novel Structure Solving Problem of Prior Art is Evidence of Un-obviousness

As argued in A1, A2, and A3 (incorporated herein by reference) at least one element of applicant invention is not disclosed in the prior art. Lack of the element in the prior

art makes the structure recited in Claims 1, 13 and 3 novel.

In addition, the novel structure provides a solution (Page 2 lines 7-11 applicants specification) to a problem discussed at page 1, line 11 to page 2 line 7 applicants specification.

It is applicants contention the novel structure provides the stated solution which solve a problem of the prior art are evidence of un-obviousness.

A9. Patentability of Claim 13

Claim 13 due to dependency on Claim 1, is patentable over the art of record, for reasons set forth above.

In addition, Claim 13 is separately patentable. Claim 13 calls for the first group of buffers and the UTOPIA interface to be positioned in the ATM clock domain and the SONNET framer processes and second group of buffers to be placed in SONNET clock domain.

The Examiner admits Seawright (US Patent 5,920,711) the primary reference does not teach this feature of applicants invention and relied upon M. Koziotis et al. for teaching this feature.

First applicants contention combining the teachings of Seawright with that of Koziotis et al. would distroy the invention on which Seawright is based. In fact it would probably render Seawright inoperable. Seawright discloses a system that generates virtual circuit based upon frame protocol inserted from GUI. The system provides an

interface called "SIMPLUG" that enable simulation. There is no teachings or suggestion of changing from ATM protocol to SONNET.

Koziotis et al. article teaches an ATM-SDH/SONET Framer IC in which ATM cells are converted to SONET Frame format and vice versa.

It is applicants contention converting a protocol into a virtual circuit does not require ATM/SONET protocol conversion. Therefore, modifying Seawright by the teachings of Koziotis would make Seawright unsuitable for its intended purpose. As a consequence, Claim 13 is separately patentable.

Furthermore, applicants argue Koziotis teaches away from Seawright in that Koziotis teaches protocol conversion ATM to SONET whereas Seawright teaches generation of virtual circuits for simulation, synthesizing etc. An artisan (one of ordinary skill in relevant art) viewing the teachings would not form a combination that would render Claim 13 obvious. As a consequence the "teach away" is an indicia of non obviousness.

A10. Patentability of Claim 17

Claim 17, due to dependency on Claim 1 is patentable for reasons set forth above supporting Patentability of Claim 1 and incorporated herein by references.

In addition Claim 17 is separately patentable. The claim calls for the format translator converts ATM cells to SONET packets and visa versa.

The references combined are in Seawright et al.(SE) (US Patent 5,920,711), Kim's

article (Design Simulation of Three ATM ASICS) and Koziotis article (ATM - SDH/SONET Framer).

As argued under A8, incorporated herein by reference, modifying Seawright as thought by Koziotis would render Seawright inoperable. The Kim article relates to ATM. It does not correct the problem of making Seawright operable when modified by the teachings of Koziotis. As a consequence the Examiner fails to make out a prima facia case of obviousness. Therefore, Claim 17 is patentable over the art of record.

Applicant is aware of the Examiners argument as basis for the combination set forth under 6.4 of the Final Office Action. It is applicants contention the argument appears complex and difficult to understand. Using the argument as basis for the combination would be outside the realm of one skilled in the art (an Artisan). Therefore, the complexity of the argument should be construed as evidence of non-obviousness of Claim 17.

B. Patentability of Claim 2

Claim 2, due to dependency on Claim 1, is patetenable for reasons set forth above and incorporated herein by references.

In addition, the claim is separately patentable because it calls for a SONET line rate of 155.52 Mbps (OC-3), 622.08 Mbps (OC-12), 2488.32 Mbps (OC-48) and model that offer sufficient parameters which can be programmed to represent Framers from different vendors. (Underlined portion of claim based upon its dependency on Claim 1). The underlined feature is not found or suggested in any of the seven (7)

references combined by the Examiner.

The programmability feature, variable line rates at least one receiver interface and at least one transmitter interface to the SONET network together makes the model recited in Claim 2 configurable to allow testing with framers from multiple vendors. (See page 2, lines 15-19; page 6, lines 25-page 7, lines 1010, applicants specification)

Because none of the cited references teaches or suggest the programmable feature of Claim 2, the chained structure is novel. The behavioural model provided by Claim 2 was not available and solve a problem for user. In fact the solution offered by the prior art were not satisfactory and create other problems (See page 1, lines 10-page 2, line 10 applicants specification). It is applicants contention the novel structure and solution of problem are evidence of non obviousness.

C. Patentability of Claim 6

Claim 6, due to dependency on Claim 1, is patentable over the art of record for reasons set forth above and incorporated herein by references. .

In addition, Claim 6 is separately patentable. Claim 6 set forth the programmable features which offers stability and allows the framer to provide different characteristics associated with framers from different manufactures. These features make the structure of Claim 6 novel. In addition, as argued under A10 and incorporated herein by reference, the novel structure solve prior art problems. Moreover, providing characteristics associated with framers from different manufactures bestow a benefit on users. It is applicants contention novel structure

with benefits and /or novel structure solving prior art problem are evidence of non-obviousness. As a consequence Claim 6 is patentable over the art of record.

It is noted the Examiner combine ten (10) references to make Claim 6 obvious. It is applicants contention an artisan viewing these references without hindsight of applicants' invention would not form the combination due to the diversity of the references. In addition, the argument is put forth by the Examiner to support the rejection appears too complex for an artisan to pursue in forming the combination. The complexity of the arguments and large number of references should be construed as evidence of un-obviousness.

D. Patentability of Claims 14-16

Claim 14-16 are rejected under 35 U.S.C 103 (a) as being unpatentable over Seawright et al. (US Patent 5,920,711) in view of Kim et al. (IEEE, August 1999 article) and Koziotis et al. (IEEE, October 1999 article) and further in view of Kim et al (US Patent 9,978,377).

In reviewing the Examiners argument, it appears as if the Examiner erred in construing Seawright et al (US Patent 5,920,711) and Kim et al. (IEEE, August 1999 article).

D1. <u>Seawright Does Not Teach "Providing a Customized Behavioural Model of an ATM/SONET Framer</u>

Claim 14, a method, in part calls for "providing a customized behavioural model of an ATM/SONET Framer..."

The Examiner argues Seawright teaches the element of Claim 14.

The Applicants argue Seawright does not teach or suggest this element. Instead, Seawright provides a system for specifying synthesizing analysis, simulating and generating circuit design from frame protocol. (Abstract). In particular, a GUI allows a user to specify, edit, browse a frame protocol which the system converts into a virtual circuit. The system also provide SIMPLUG, an interface, that couples the virtual circuit to a simulation. No part of this reference suggest or teach an ATM/SONET Framer. Therefore, the Examiner's conclusion appears to be in error.

D2. Kim et al. IEEE, August 1999 Article Does not Teach " Providing Software Which Include Sufficient Programmable Parameters for Representing Framers from Different Vendors"

Claim 14, second element in part calls for "... said software including sufficient programmable parameters for representing framers from different vendors." In addition, Claim 14 (last element) calls for activating selected ones of said programmable parameters .....

The Examiner relied on Kim et al. article to teach both elements of Claim 14 (See page 15, last paragraph of Final Rejection, paper # 9). Applicants contend Kim et al. article does not teach or suggest either one of the two elements. Instead Kim et al., teaches design and simulation of three ATM ASICS, includes UTOPIA transmit (Tx)

and Receiver (Rx) interfaces. (Figure 3 and associated description, Kim et al. article.) Therefore, the Examiners construction of Kim et al. article appears to be in error.

D3. Novel Process and Benefits Suggest Non Obviousness

As argued above and incorporated herein by reference at least one element of applicants' Claim 14 is not disclosed or suggested in the cited references. As a consequence Claim 14 provide a novel method. The method calls for providing software with sufficient programmable parameters to represent framers from different manufacture. This bestows a benefit in that a single framer, as opposed to a plurality of framers (one from each manufacture), is required. This also has reduce cost in, that one programmable framer cost less than a plurality.

It is applicants contention a novel method and benefits are indicia of non-obviousness. Therefore, Claims 14-16 are patentable over the art of record.

D4. Novel Process and Solution to Prior Art Problem are Evidence of Non Obviousness

As argued above and incorporated herein by references, the process or method of Claim 14 is novel.

As set forth in applicants specification at page 1, line 10 through page 2, lines 1-10 this prior art has a problem with inadequate solution suggested to solve the problem (see applicants' specification, page 1, lines 1-20). The method of applicants' Claim

14 solves the problem.

It is applicants contention novel process and solution to problem are evidence of non-obviousness.

In addition, applicants argue the problem (see applicant's specification, page 1 line 10 through page 2, line 1-10) which Claim 14 addresses is different from problems addressed by the references cited by the Examiner.

It is applicants contention Novel process steps and solutions to different problems are further evidence of non-obviousness.

D5. Prima Facia Case of Obviousness Has Not Been Made

In rejecting claims under 35 U.S.C 103 (a) the Examiner is obliged to make out a prima facia case of obviousness. This requires that every element of the rejected claim be found in the combination of references. As argued above and incorporated herein by reference at least one element of Claim 14 is not present or suggested in the Examiner's combination. Therefore, a prima facia case of obviousness has not been made.

Another criteria for making out a prima facia case of obviousness is there must be some suggestion or motivation to combine found in teachings of at least one of the references. None (motivation to combine) could be found in the present case and the Examiner has not point to suggestion or motivation in any of the references. Instead, the Examiner made arguments (see 9.1, 9.2 and 9.3, pages 14-18, Final Office Action, paper # 9) as basis for the combination. Arguably, such arguments, if

concrete logical and within the skill of one skilled (an artisan) in the art, could support an obviousness rejection.

However, it is applicants contention the Examiner's arguments do not appear to be concrete and logical to support findings of obviousness. In addition, as argued above and incorporated herein by reference, the arguments appear to fall outside the knowledge of an artisan. As a consequence such arguments cannot be used to justify a finding of obviousness. In addition, applicants argue an artisan viewing the references would not form the combination because the references relates to different inventions. For example Seawright et al. (US Patent 5,920,711) teaches generating a virtual circuit based upon specified protocols manipulated via GUI. Kim et al. (IEEE, August 1999) article describes design and simulation of three ATM ASICS. There is no reason to combine these two references especially since they refer to different inventions.

Moreover, combining these two references would require modification of Seawright in such a way to make it unsuitable for the purpose for which it was invented. This type of modification suggests lack of motivation or suggestion to combine.

In view of the above Claims 14-16 are not obvious.

D6. PATENTABILITY of Claim 15

Claim 15, due to dependency on Claim 14, is patentable over art of record.

In addition, Claim 15 is separately patentable. Claim 15 due to dependency on Claim 14 calls for providing sufficient programmable parameters for representing

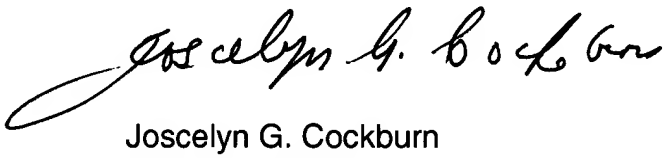
frames from different vendors and for causing the model to operate at different line rates.

It should be noted " different line rates" and framers from different vendors are different desirable functions, requiring different parameters. The presence of these functions in a single model provides advantages (see page 8, line 21 through page 7, lines 1-20, applicants specification) which are evidence of non obviousness. Therefore, Claim 15 is separately patenable.

CONCLUSION

In view of the arguments and facts set forth herein the appended Claims define patentable subject matter and are not made obvious by the cited prior art. As a consequence the final rejection of Claims 1,2,3,6 and 13-17 should be reversed.

Respectfully submitted,



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Appendix of Rejected Claims:

1. A computer based system employing a customizable Simulation Model of an ATM/SONET Framer, for system level verification and performance characterization, comprising:

means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors;

a Receiver system;

a Transmitter system wherein said Receiver system and said Transmitter system are independently configurable and each includes a UTOPIA interface programmable to provide different protocols;

a first group of buffers operatively coupled to the UTOPIA interface;

SONET Framer Processes including a format translator; and

a second group of buffers operatively coupled to the SONET Framer Processes.

2. The system of claim 1 wherein said ATM/SONET Framer provides at least one Receive and at least one Transmit interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08 Mbps(OC-12) and 2488.32 Mbps(OC-48).

3. The system of claim 13 wherein said ATM clock domain and said SONET clock domain operate on different clock frequencies and represent two distinct clock domains.

6. The system of claim 1 which in addition, offers programmability, rich feature

set, and two independently configurable models, one each for said transmit side and said receive side, and

offers said programmability features of:

- SONET line rates (OC-Nc: N=1..48; OC-1=51.48 Mbps)
- Percentage of data bytes vs. overhead bytes per row
- Delays associated with clock domain synchronization
- FIFO depth and threshold (in terms of number of cells)
- Byte or word count threshold within a cell associated with FIFO status update
- UTOPIA Level-2/3
- Built-in performance checking

13. The computer base system of claim 1 wherein the first group of buffers and the Utopia interface are positioned in an ATM clock domain and the SONET Framer Processes and the second group of buffers are placed in a SONET clock domain.

14. A computer base method for system level verification and performance characterization comprising:

providing a customized behavioral model of an ATM/SONET Framer which includes independently configurable Receiver system and Transmitter system;

providing software for coacting with said behavioral model, said software including sufficient programmable parameters for representing Framers from different vendors; and

activating selected ones of said programmable parameters which cause the model to behave as a framer from a particular framer manufacturer.

15. The method of claim 14 further including providing additional parameters, that causes the model to operate at different line rates.

16. The method of claim 15 further including activating selected ones of the additional parameters to cause the model to operate at one of a plurality of line rates.

17. The computer based system of claim 1 wherein the format translator converts ATM cells to SONET packets and visa versa.